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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,386	10/02/2006	Gunther Leising	00366.000214.	1805
5514 7590 05/27/2010 FITZPATRICK CELLA HARPER & SCINTO 1290 Avenue of the Americas NEW YORK, NY 10104-3800				
EXAMINER				
LI MEIYA				
ART UNIT		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary**Application No.**

10/586,386

Applicant(s)

LEISING, GUNTHER

Examiner

MEIYA LI

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Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 3/8/10.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 9-15 is/are pending in the application.
- 4a) Of the above claim(s) 11 and 14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 9, 10, 12, 13 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SI/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Interval Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Applicant's request for reconsideration of the rejection of the last Office action is persuasive and, therefore, the rejection of that action is withdrawn.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "light emitting diode die is mounted face down on the light emitting diode printed circuit board" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Hashemi et al. (2002/0149102).

As for claim 9, Hashemi et al. in Fig. 1 and related text a light emitting diode 100, comprising:

at least one light emitting diode die 110, arranged on a light emitting diode printed circuit board (conductive layers 138/114/132/144/148/146 sandwiched between an insulating layer 120) by means of a die attach 112, the light emitting diode printed circuit board comprising at a lower surface 124 thereof rear side contacts 144/146/148, wherein the rear side contacts at least partially overlap with contours of the light emitting diode die and are formed in such a way as to overlay with at least half of the lower surface of the printed circuit board, and

wherein the printed circuit board comprises a plurality of through-contacts 126/128/130 thermally and electrical connecting the rear side contacts to contact areas formed on an upper surface 118 of the printed circuit board.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi et al. (2002/0149102) in view of Hoelen et al. (2002/0167016).

Hashemi et al. disclosed substantially the entire claimed invention, as applied to claim 9 above, except the light emitting diode printed circuit board is a metal core printed circuit board, and wherein the light emitting diode die is located on the metal core.

Hoelen et al. teach the light emitting diode printed circuit board is a metal core printed circuit board, and wherein the light emitting diode die is located on the metal core ([0178]).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to use metal core printed circuit board, as taught by Hoelen et al., in Hashemi et al.'s device, in order to provide a better heat dissipation and improve the performance of the device.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi et al. (2002/0149102) in view of Shimizu et al. (2003/0189829).

Hashemi et al. disclosed substantially the entire claimed invention, as applied to claim 9 above, except the light emitting diode die is mounted face down on the light emitting diode printed circuit board.

Shimizu et al. teach in Fig. 5b and related text the light emitting diode die 2 is mounted face down on the light emitting diode printed circuit board 1.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to mount the light emitting diode die face down on the light emitting diode printed circuit board, as taught by Shimizu et al., in Hashemi et al.'s device, in order to utilize the total chip area to make the I/O connections, and increases productivity and simplifies the manufacturing process.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi et al. (2002/0149102) and Hoelen et al. (2002/0167016), in view of Shimizu et al. (2003/0189829).

Hashemi et al. and Hoelen et al. disclosed substantially the entire claimed invention, as applied to claim 10 above, except the light emitting diode die is mounted face down on the light emitting diode printed circuit board.

Shimizu et al. teach in Fig. 5b and related text the light emitting diode die 2 is mounted face down on the light emitting diode printed circuit board 1.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to mount the light emitting diode die face down on the light emitting diode printed circuit board, as taught by Shimizu et al., in Hashemi et al. and Hoelen et al.'s device, in order to utilize the total chip area to make the I/O connections, and increases productivity and simplifies the manufacturing process.

8. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashemi et al. (2002/0149102) and in view of Durocher et al. (6,614,103).

As for claim 13, Hashemi et al. in Fig. 9 and related text a light emitting diode light source comprising:

at least one light emitting diode, wherein each said diode comprises at least one light emitting diode die 910/912, arranged on a light emitting diode printed circuit board (conductive layers 922/938/980/966/943/967/949 sandwiched between an insulating layer 920) by means of a die attach 904/908, the light emitting diode printed circuit board comprising at a lower surface 925 thereof rear side contacts 943/949/967, wherein the rear side contacts at least partially overlap with contours of the light emitting diode die and are formed in such a way as to overlap with at least half of the lower surface of the printed circuit board, and wherein the printed circuit board comprises a plurality of through-contacts 927/929/939/941 thermally and electrical connecting the rear side contacts to contact areas formed on an upper surface 918 of the printed circuit board, said diode being arranged on an additional board 998,

wherein the additional board comprises on an upper surface thereof further contact areas which are soldered 951/957/969 to the rear side contact of the light emitting diode,

wherein a total surface area of the further contact areas is at least half of the area of the lower surface of the light emitting diode printed circuit board.

Hashemi et al. do not disclose the additional board comprises a further plurality of through-contacts thermally and electrically connecting at least one of the further contact areas to a solder area formed at a lower surface of the additional board.

Durocher et al. teach in Fig. 4 and related text the additional board 41 comprises a further plurality of through-contacts 51 thermally and electrically connecting at least one of the further contact areas to a solder area 47 formed at the bottom 45 of the additional board.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to form a further plurality of through-contacts thermally and electrically connecting at least one of the further contact areas to a solder area formed at a lower surface of the additional board, as taught by Durocher et al., in Hashemi et al.'s device, in order to provide a better heat dissipation and improve the performance of the device.

As for claim 15, Hashemi et al., and Durocher et al. disclosed substantially the entire claimed invention, as applied to claim 13 above, except at least one of the plurality of through-contacts of the diode and at least one of the further plurality of through-contacts of the additional board have a diameter of less than 100 μm .

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to at least one of the plurality of through-contacts of the diode and at least one of the further plurality of through-contacts of the additional board having a diameter of less than 100 μm , in order to optimize the performance of the device. Furthermore, it has been held that discovering an optimum value of a result

effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

It has been held in that the applicant must show that a particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Note that the law is replete with cases in which when the mere difference between the claimed invention and the prior art is some dimensional limitation or other variable within the claims, patentability cannot be found. The instant disclosure does not set forth evidence ascribing unexpected results due to the claimed dimensions. See *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338 (Fed. Cir. 1984), which held that the dimensional limitations failed to point out a feature which performed and operated any differently from the prior art.

Response to Arguments

9. Applicant's arguments with respect to claims 9, 10, 12, 13 and 15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MEIYA LI whose telephone number is (571)270-1572. The examiner can normally be reached on Monday-Friday 8:00AM-4:30PM Eastern Standard Time.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art
Unit 2811

/M. L./
Examiner, Art Unit 2811
12/5/2009